AF/2661

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	Martin *et al.*	Examiner:	Moore, I.
Serial No.:	09/662,077	Group Art Unit:	2661
Filed:	September 14, 2000	Docket No.:	8X8S.243PA
Title:	Voice-Over Internet Protocol Processor		

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence and the papers, as described hereinabove, are being deposited in the United States Postal Service, as first class mail, in an envelope addressed to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on Monday, January 9, 2006.

By: Kelly S. Waltigney
Kelly S. Waltigney

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Customer No.
40581

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed November 8, 2005 and in response to the final rejection of Claims 1-18 and 20-28 as set forth in the final Office Action dated August 9, 2005.

Please charge Deposit Account number 50-0996 (8X8S.243PA) in the amount of $500.00 for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 (8X8S.243PA) additional fees/overages in support of this filing.

01/12/2006 EAREGAY1 00000076 500996 09662077
01 FC:1402 500.00 DA

I. Real Party In Interest

The real party in interest is 8x8, Inc., formerly Netergy Microelectronics, Inc., having a principal place of business at 2445 Mission College Boulevard, Santa Clara, CA 95054. The above-referenced patent application is assigned to 8x8, Inc.

II. Related Appeals and Interferences

Appellant is unaware of any related appeals or interferences.

III. Status of Claims

Claims 1-18, 20-22 and 24-28 stand rejected and are presented for appeal; the pending claims under appeal are listed in the attached Claims Appendix, with claims cancelled and indicated allowable reflected accordingly.

IV. Status of Amendments

No amendments have been filed subsequent to the Final Office Action mailed on August 9, 2005.

V. Summary of Claimed Subject Matter

The present invention is directed to processing voice data over an Internet protocol (IP) network. The present invention is exemplified in a number of implementations and applications, some of which are summarized below.

An example embodiment of the present invention is directed to the integration of several functions into a single chip that implements programmable controller and compression applications in software architecture with standard C programmability. *See, e.g.*, FIGs. 1 and 2 and corresponding discussion at page 7, line 18 through page 8, line 10, with further supporting discussion made in connection with FIGs. 3-7. The device exhibits low-power consumption and a compact physical size realized by integrating sufficient memory on the chip to implement functions required by a thin-client, connection-less IP telephony device. *See, e.g.*, page 12, lines 7-17.

According to another example embodiment of the present invention, a programmable audio processor chip for processing voice data is adapted to process voice data using IP communications using low power and maintaining a compact configuration. *See, e.g.*, FIGs. 1, 2 and discussion at page 7, line 18 through page 8, line 10, and at page 11, line 20 through page 12, line 6. The chip includes a voice compression device, audio processing circuitry, an IP network stack and a communication stack. *See, e.g.*, FIGs. 3 and 4 and corresponding discussion at page 8, line 11 through page 10, line 17. The circuitry is programmed with an audio processing software application for processing compressed voice data. *See, e.g.*, FIGs. 1-4 and discussion at page 9, line 10 through page 10, line 9. The communication stack is adapted to store and process communications data including protocol data for communicating the voice data. *See, e.g.*, FIGs. 3&4 and corresponding discussion at page 8, line 11 through page 10, line 17. The chip processes the voice data using the IP stack to communicate via an IP network. *See, e.g.*, FIGs. 1, 7 and 11 and corresponding discussion at page 7, line 18 through page 8, line 10.

According to another example embodiment of the present invention, a telephony communications device is adapted to communicate data including voice data. The device includes a programmable audio processor chip having both microcontroller and DSP functions and adapted to perform Internet protocol/digital (IP/D) conversions for IP voice data and digital voice data, wherein the programmable audio processor chip includes an IP network stack and a communications stack. *See, e.g.*, FIGs. 1, 2 and discussion at page 7, line 18 through page 8, line 10, and at page 11, line 20 through page 12, line 6. *See also, e.g.*, FIGs. 3&4 and corresponding discussion at page 8, line 11 through page 10, line 17. An audio capture device is communicatively linked to the programmable audio processor chip and adapted to capture a voice signal and communicate the captured voice signal to the programmable audio processor chip. *See, e.g.*, page 4, line 16 through page 5, line 4, and FIGs. 10, 11 and 12. An audio speaker is communicatively linked to the programmable audio processor chip and adapted to generate sound in response to a signal communicated from the programmable audio processor chip. *See, e.g.*, page 4, line 16 through page 5, line 4, and FIGs. 10, 11 and 12.

According to another example embodiment of the present invention, an IP telephony communications network includes a plurality of IP telephony devices (*see, e.g.*, FIG. 11) each having a programmable audio processor chip. *See, e.g.*, FIGs. 1, 2 and discussion at page 7, line 18 through page 8, line 10, and at page 11, line 20 through page 12, line 6. The programmable audio processor chips each include a DSP voice compression device adapted to compress the voice data, audio processing circuitry programmed with an audio processing software application for processing the compressed voice data, an IP network stack adapted to store and process IP data, the IP network stack including protocols for processing the compressed voice data via an IP network, and a communication stack adapted to store and process communications data, the communications stack including audio processing protocols for processing the compressed voice data. *See, e.g.*, FIGs. 3&4 and corresponding discussion at page 8, line 11 through page 10, line 17. *See also, e.g.*, FIGs. 3&4 and corresponding discussion at page 8, line 11 through page 10, line 17. The IP telephony communications network further includes a CPU adapted to communicate with the plurality of IP telephony communications devices and to program the programmable audio processor chip in each IP telephony device, the programming including communications protocols, the CPU having a standard RISC 5-stage pipeline adapted to execute a plurality of instructions simultaneously. *See, e.g.*, FIG. 1 and page 7, line 18 through page 8, line 10. A communications link is coupled to each of the IP telephony devices and to the CPU and is adapted to transmit communications data including voice IP data. *See, e.g.*, FIGs. 11 and 12, and page 11, lines 8-19.

According to another example embodiment of the present invention, a programmable audio processor chip processes telephony voice data. The chip includes a DSP voice compression and decompression device adapted to compress and decompress the telephony voice data, a programmable processing layer programmed with an audio processing application for processing the compressed telephony voice data, an IP network stack adapted to store and process IP telephony data, the IP network stack including protocols for processing the compressed telephony voice data via an IP network, and a communication stack adapted to store and process communications data, the communications stack including

audio processing protocols for processing the compressed voice data. *See, e.g.*, FIGs. 3&4 and corresponding discussion at page 8, line 11 through page 10, line 17. *See also, e.g.*, FIGs. 3&4 and corresponding discussion at page 8, line 11 through page 10, line 17.

VI. Grounds of Rejection to be Reviewed Upon Appeal

1. Claims 1-8, 13, 14, 24 and 25 stand rejected under 35 U.S.C. § 103(a) over Edholm (U.S. Patent No. 6,449,269) in view of Dean *et al.* (U.S. Patent No. 5,303,326).

2. Claim 9 stands rejected under 35 U.S.C. § 103(a) over Edholm in view of Dean *et al.* as applied to claim 1 above, and further in view of Sugiura *et al.* (U.S. Patent No. 4,248,200) and Waggoner *et al.* (U.S. Patent No. 6,218,706).

3. Claim 10 stands rejected under 35 U.S.C. § 103(a) over Edholm and Dean *et al.* as applied to claim 1 above, and further in view of Bertin *et al.* (U.S. Patent No. 6,097,243).

4. Claims 11 and 26-28 stand rejected under 35 U.S.C. § 103(a) over Edholm and Dean *et al.* as applied to claims 1 and 25 above, and further in view of Mason *et al.* (U.S. Patent No. 6,727,451).

5. Claims 12 and 15-18 stand rejected under 35 U.S.C. § 103(a) over Edholm and Dean *et al.* as applied to claims 1 and 13 above, and further in view of Maeda *et al.* (U.S. Patent No. 5,884,074).

6. Claim 20 stands rejected under 35 U.S.C. § 103(a) over Edholm in view of Dean *et al.*, and further in view of Dean (U.S. Patent No. 5,553,276).

7. Claims 21-22 stand rejected under 35 U.S.C. § 103(a) over Edholm and Dean '326 as applied to claim 20 above, and further in view of Adelman (U.S. Patent No. 5,598,362).

VII. Argument

Appellant notes that the Final Office Action failed to address Appellant's arguments, while repeating the previous rejections in a manner contrary to MPEP § 707.07(f) and 35 U.S.C. §132. Specifically, the Examiner has not addressed Appellant's arguments directed toward the Examiner's incorrect interpretations of the primary '269 reference (upon which all claim rejections rely) as indicated in the Office Action Response filed June 28, 2005. While Appellant recognizes that this failure to comply with the MPEP is not an issue available for appeal, Appellant requests that the issues outlined below be reviewed in light of this lack of compliance as the Appellant has been denied the opportunity to judge the propriety of the Section 103(a) rejections and respond thereto. Appellant has highlighted certain aspects of these interpretations below; Appellant believes the resolution of these incorrect interpretations with accurate interpretations renders all of the rejections improper.

1. The rejection of claims 1-8, 13, 14, 24 and 25 fails because the primary '269 reference does not correspond to the claimed limitations, the Examiner's allegations of inherency in modifying the '326 reference are unsupported by any evidence, and the proposed modification would render the '269 reference unsatisfactory for its intended purpose.

The Section 103 rejection should be reversed because the '269 reference does not teach or suggest a programmable audio processor chip as asserted by the Examiner and as claimed in the instant application. Relevant claimed limitations include, for example, a single chip having an IP network stack, a communication stack, a DSP voice compression device adapted to compress voice data and audio processing circuitry programmed with an audio processing software application for processing the compressed voice data. These claimed limitations are directed to inventive aspects that have been found particularly useful in applications benefiting from such a single-chip application, such as those benefiting from small size and/or low power consumption. The cited references, alone or in combination, do not show this combination of limitations as implemented on a single chip, the cited portions of the '269 reference do not correspond to the claimed limitations, and the Examiner has not

shown how the proposed combination of disparate portions onto a common chip could be achieved. Furthermore, Appellant has provided the Examiner with evidence showing the impropriety of the Examiner's assertions of correspondence between various portions of the primary '269 reference and the claimed limitations. In this regard, the cited references not only fail to show all of the claimed limitations, they also fail to describe how the Examiner's proposed combination/modification of components by integrating them into a single chip would function. In the following, specific focus is given to claimed limitations directed to an IP network stack and to a communications stack, to which the cited portions of the '269 reference fail to correspond.

Beginning with claimed limitations directed toward an IP network stack, the Examiner cited a "system of Packetizer 334, memory 332, and Extractor 322" in an attempt to read the '269 reference upon the claimed limitations; the Examiner further cited the same Packetizer 334 and memory 332, combined with a Controller 314, as corresponding to a communication stack. In an attempt to combine these different portions of the '269 reference, the Examiner further alleged that "stacks or layers, as it well know [sic] in the art, are basically software application/codes/process" that correspond to (claimed limitations) including an "IP network stack" and a "communications stack." The Examiner also alleged that "it is clear that the IP network stack and a communication stack are software components/codes, which can be embodied anywhere." Appellant submits that these assertions are not only improper in view of well-known art, they lack evidentiary support and fail to show how the portions of the '269 reference would function as claimed and would further be combined as suggested in order to correspond to the claimed limitations.

In attempting to support the assertion that the '269 reference teaches an IP network stack as claimed, the Examiner provided the following discussion as indicated in the Final Office Action:

> Edholm's combined system of Packetizer 334, memory 332, and Extractor 322 has a functionally [sic] of IP network stack software/method/processes. Another [sic] word, IP network stack is embodied in a combined system of Packetizer 334, memory 332, and Extractor 322 since they both have identical functionality.

However, the Examiner's conclusion that the IP network stack and the "Packetizer 334, memory 332, and Extractor 322 ... have identical functionality" is wholly unsupported and incorrect. Specifically, Packetizer 334 communicates bi-directionally with memory 332, and extractor 322 communicates bi-directionally with memory 332. *See* Fig. 3. For example, at column 6, line18, the '269 reference indicates that packetizer 334 communicates bi-directionally with memory where it states "[t]he packetizer then queries memory 332 for the desired destination IP address . . . and builds an IP packet header information using at least one of the returned destination IP addresses." Therefore, the Packetizer 334, memory 332, and extractor 322 of the '269 reference fail to correspond to Appellant's IP network stack as claimed.

The Examiner's above discussion relative to the claimed IP network stack also stops short of showing how the combination of packetizer, memory and extractor would be implemented with the functionality as alleged by the Examiner. For example, the Examiner cited no evidence from the '269 reference or the prior art that suggests that such components could be implemented in an IP network stack, much less on a common chip. Further, if the Examiner is asserting (as apparently so) that all of these functions (packetizer 334, memory 332, extractor 322) are software-embodied functions, it is unclear as to how such functions would operate in accordance with an IP stack as claimed, and how the '269 reference would accordingly function.

Referring again to page 26 of the Final Office Action, the Examiner's alleged support for asserting that the '269 reference teaches a communications stack as claimed is directed to the following:

> Edholm's a [sic] combined system of Controller 314, Packetizer 334 and memory 332 has a functionally [sic] of communication network stack software/method/processes. Another [sic] word, communication stack is embodied in a combined system of Controller 314, Packetizer 334 and memory 332 since they both have identical functionality.

As with the discussion above, the Examiner's conclusion that the "combined system of controller 314, packetizer 334, and memory 332," have identical functionality with the claimed communications stack is unsupported and incorrect. For example, memory 332

exports data and receives data from packetizer 334 and from controller 313. *See* Fig. 3. Because memory receives and exports data to both controller 314 and packetizer 334, the combined system of controller 314, packetizer 334, and memory 332 do not operate as a stack where each layer only uses functions of the layer below, and only exports functionality to the layer above. Therefore, the Controller 314, Packetizer 334 and memory 332 of the '269 reference fail to correspond to Appellant's communication stack as claimed.

The Section 103 rejections are also improper because the Examiner failed to cite any evidence from the prior art in support of modifying the various portions of the '269 reference to arrive at claimed limitations such as an IP network stack and a communications stack. For instance, the Examiner's apparent attempt to characterize the various components (*e.g.*, packetizer 334, memory 332, extractor 322 and controller 314) of the '269 reference as "software" and/or an "IP network stack" or "communication stack" is a modification of the '269 reference that requires supporting evidence from the prior art. However, no such evidence was cited. Instead, the Examiner has made broad conclusory statement, alleging that such a modification is well-known and, apparently, that such a modification would inherently be implemented on a common chip. Without evidence from the prior art, Appellant submits that such allegations made with a hindsight view of the instant invention are improper and fail to establish a *prima facie* case of obviousness.

In further regard to the Examiner's assertions of identical functionality and apparent inherency-type allegations, Appellant submits that such inherency-type assertions must be established by intrinsic evidence from the prior art, yet no such art has been provided. Specifically, to establish inherency, extrinsic evidence "must make clear that the missing descriptive matter *is necessarily present in the thing described in the reference*, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 U.S.P.Q.2d 1746, 1749 (Fed. Cir. 1991) (emphasis added). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *Id.* at 1269, 20 U.S.P.Q.2d at 1749 (quoting *In re Oelrich*, 666 F.2d 578, 581, 212 U.S.P.Q. 323, 326 (C.C.P.A. 1981). In this instance, the Examiner's assertion that the Packetizer 334,

memory 332, and Extractor 322 are an IP network stack and that the Controller 314, Packetizer 334 and memory 332 are a communication stack relies upon such an inherency-type assertion and is unsupported by any intrinsic evidence. Furthermore, Appellant asserts that such a combination is not inherent because the Packetizer 334, memory 332, Extractor 322 and Controller 314 do not function in accordance with a stack as discussed above.

In addition to the above, the Examiner's proposed modification of the various components (*e.g.*, packetizer 334, memory 332, extractor 322 and controller 314) of the '269 reference would appear to undermine the purpose of the '269 reference, including that directed to bi-directional communication as discussed above. Such bi-directional communication is in apparent contrast with the Examiner's assertion that such components are part of an IP network stack or communications stack. Relevant case law indicates that, where a proposed modification of a primary reference would undermine the purpose of that reference, the modification is unmotivated. *See, e.g., In re Gordon*, 733 F.2d 900, 221 U.S.P.Q. 1125 (Fed. Cir. 1984) (A §103 rejection cannot be maintained when the asserted modification undermines purpose of main reference).

In view of the above, all of the claim rejections are improper because each relies upon the primary '269 reference and the (improperly) alleged teachings therein, alone or in connection with other references, and because the Examiner has failed to cite evidence in support of the proposed modification of the '269 reference. The above arguments thus apply to other grounds of rejection discussed below. In this regard, the rejections of claims 1-8, 13, 14, 24 and 25 as discussed above, as well as the rejections of the remaining claims discussed below, should all be reversed.

2. The rejection of claim 9 should be reversed for the reasons stated above in connection with the first ground of rejection and further because the Examiner's suggestion that the chip of the '269 reference can operate as claimed simply because other chips can, without any supporting evidence, is untenable.

As claim 9 depends from claim 1, Appellant submits that the discussion above with the first ground of rejection applies to claim 9 here, with the relevant portion of that discussion omitted for brevity. "If an independent claim is nonobvious under 35 U.S.C. §

103, then any claim depending therefrom is nonobvious." MPEP § 2143.03; *citing In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

In addition to the above, the Examiner has acknowledged that the '269 and '326 references fail to teach or suggest limitations directed to a programmable audio processor chip adapted to dissipate 250 mW at 200 MHz. In an attempt to add these limitations to the primary '269 reference, the Examiner has cited two new references (the '200 and '706 references) as chips that can respectively dissipate 250 mW or operate at 200MHz. In short, the Examiner cited two references apparently disclosing integrated circuits that simply happen to operate under such conditions, without showing how such operation could be achieved with the combined components of the '269 and '326 reference.

Furthermore, the cited '200 and '706 references appear unrelated to the claimed limitations, in that the '200 reference is directed to an internal combustion engine, and that the '706 reference is directed to an electrostatic discharge protection circuit. In this regard, Appellant submits that one of skill in the art would not be motivated to combine the references as suggested, and further that the Examiner provided no evidence suggesting that such combination would be motivated.

In view of the above, the rejection of claim 9 is further improper because the Examiner's simple recitation of an IC that happens to operate under certain conditions stops short of teaching an enabling approach to the claimed limitations in the prior art, and because the proposed modification of the '269 reference is unmotivated. Therefore, Appellant submits that the rejection of claim 9 must also be reversed.

3. The rejection of claim 10 is improper for the reasons stated above in connection with the first ground of rejection, because the cited references do not teach or suggest the claimed limitations, and because the proposed modification of the '269 reference is unlikely to succeed and thus unmotivated.

As claim 10 depends from claim 1, Appellant submits that the discussion above with the first ground of rejection applies to claim 10 here, with the relevant portion of that discussion omitted for brevity. "If an independent claim is nonobvious under 35 U.S.C. §

103, then any claim depending therefrom is nonobvious." MPEP § 2143.03; *citing In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

In addition to the above, Appellant submits that the Examiner's attempt to arrive at the claimed limitations by citation to the '243 reference stops short of teaching or suggesting claimed limitations directed to audio processing circuitry programmed with a power-down mode, wherein the internal clock frequency is slowed during periods of chip inactivity. That is, the Examiner has simply cited a "groggy mode" of the '243 reference without any explanation as to how such a groggy mode would apply to the primary '269 reference. For example, it is unclear as to how the '243 references groggy mode would be implemented with the controller 314. Furthermore, it is unclear as to how the alleged benefits (motivation) of adding such a groggy mode to the primary '269 reference would be evident to one of skill in the art, as no such art is cited. In this regard, the Section 103 rejection of claim 10 should also be reversed because the proposed modification of the '269 reference appears unlikely to succeed and because the alleged motivation is unsupported by any evidence from the prior art.

4. The rejection of claims 11 and 26-28 is improper for the reasons stated above in connection with the first ground of rejection.

As claims 11 and 26-28 depend from claim 1 or claim 25, Appellant submits that the discussion above with the first ground of rejection applies to claims 11 and 26-28 here, with the relevant portion of that discussion omitted for brevity. "If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious." MPEP § 2143.03; *citing In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). In this regard, the Section 103 rejection of claim 11 and 26-28 should be reversed.

5. The rejection of claims 12 and 15-18 is improper for the reasons stated in connection with the first ground of rejection, and because the Examiner has failed to show how the proposed modification of the '269 reference is motivated or how the resulting combination of references could function.

As claims 12 and 15-18 depend from claim 1 or claim 13, Appellant submits that the discussion above with the first ground of rejection applies to claims 12 and 15-18 here, with the relevant portion of that discussion omitted for brevity. "If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious." MPEP § 2143.03; *citing In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

In addition to the above, the Examiner has failed to show how the flash memory approach of the '074 reference could function with the primary '269 reference. Furthermore, the alleged motivation to modify the '269 reference appears unrelated to the '269 reference. Specifically, it is unclear as to why one of skill in the art would be motivated to release "the entire area of the flash memory for a user program area" in the '269 reference. The Examiner has failed to cite any evidence from the prior art showing why such a modification of the '269 reference would be beneficial, and Appellant cannot ascertain any rationale for such a modification from the '269 reference itself. Therefore, the Section 103 rejections of claims 12 and 15-18 should also be reversed because the proposed modification of the primary '269 reference is both unlikely to succeed and unmotivated.

6. The rejection of claim 20 should be reversed for the reasons stated in connection with the first ground of rejection above, and because the proposed modification of the '269 reference is unmotivated.

As the rejection of claim 20 relies upon the modification of the '269 reference as in the first ground of rejection above, appellant submits that the discussion with the first ground of rejection above applies here.

In addition to the above, the Examiner has failed to cite evidence for alleged motivation for modifying the '269 reference. For instance, on page 22 of the Final Office Action, the Examiner discusses alleged advantages of enabling a standardized CPU to "inter-operate with the other CPU or devices" without citing any supporting evidence or discussing why such an advantage would apply to the '269 reference. In this regard, the Section 103 rejection of claim 20 should also be reversed because the rejection is unmotivated.

7. The rejection of claims 21-22 is improper for the reasons stated above in connection with the sixth ground of rejection.

As claims 21-22 depend from claim 20, Appellant submits that the discussion above with the Sixth ground of rejection applies to claims 21-22 here, with the relevant portion of that discussion omitted for brevity. "If an independent claim is nonobvious under 35 U.S.C. § 103, then any claim depending therefrom is nonobvious." MPEP § 2143.03; *citing In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore, the rejection of claims 21-22 should be reversed.

VIII. Conclusion

In view of the above, Appellant submits that the rejections of claims 1-18, 20-22 and 24-28 are improper. Appellant therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

Respectfully submitted,

CRAWFORD MAUNU PLLC
1270 Northland Drive – Suite 390
St. Paul, MN 55120
(651) 686-6633

By: _____
Name: Eric J. Curtin
Reg. No. 47,511
Robert J. Crawford
Reg. No. 32,122

CLAIMS APPENDIX
(S/N 09/662,077)

1. A programmable audio processor chip for processing voice data comprising:

a DSP voice compression device adapted to compress the voice data;

audio processing circuitry programmed with an audio processing software application for processing the compressed voice data;

an IP network stack adapted to store and process IP data, the IP network stack including protocols for processing the compressed voice data via an IP network; and

a communication stack adapted to store and process communications data, the communications stack including audio processing protocols for processing the compressed voice data.

2. The programmable audio processor chip of claim 1, wherein the programmable audio processor chip is further adapted to convert the voice data between IP audio data and digital audio data.

3. The programmable audio processor chip of claim 1, further comprising an analog-digital (A/D) converter adapted to convert the voice data between analog and digital form.

4. The programmable audio processor chip of claim 3, wherein the A/D converter is adapted to convert a voice signal captured at a microphone of a telephony device employing the programmable audio processor chip.

5. The programmable audio processor chip of claim 3, further comprising a telephony device that houses the programmable audio processor chip, wherein the A/D converter is adapted to convert digital data into analog form for use at a speaker of the telephony device.

6. The programmable audio processor chip of claim 1, wherein the IP network stack includes at least one of: a TCP/IP stack and a H.323 stack.

7. The programmable audio processor chip of claim 1, wherein the communication stack is adapted to provide at least one of the following protocols: call setup, call tear down, capabilities exchange and negotiation.

8. The programmable audio processor chip of claim 1, further comprising sufficient on-chip RAM to run a connection-less thin client call stack, a TCP/IP stack and audio compression protocols, wherein the programmable audio processor chip is adapted to function without external system memory.

9. The programmable audio processor chip of claim 1, wherein the programmable audio processor chip is adapted to dissipate 250 mW at 200 MHz.

10. The programmable audio processor chip of claim 1, wherein the audio processing circuitry is programmed with a power-down mode, wherein the internal clock frequency is slowed during periods of chip inactivity.

11. The programmable audio processor chip of claim 1, wherein the audio processing circuitry is adapted to be programmed using C programming language.

12. The programmable audio processor chip of claim 1, wherein the audio processing circuitry further comprises Flash-cache architecture adapted to enable a CPU to boot and run code from an external Flash-style device, and mix this execution space with memory on the chip.

13. A telephony communications device adapted to communicate data including voice data, the device comprising:

a programmable audio processor chip having both microcontroller and DSP functions and adapted to perform Internet protocol/digital (IP/D) conversions for IP voice data and

digital voice data, wherein the programmable audio processor chip includes an IP network stack and a communications stack;

an audio capture device communicatively linked to the programmable audio processor chip and adapted to capture a voice signal and communicate the captured voice signal to the programmable audio processor chip; and

an audio speaker communicatively linked to the programmable audio processor chip and adapted to generate sound in response to a signal communicated from the programmable audio processor chip.

14. The telephony communications device of claim 13, wherein the programmable audio chip comprises:

a DSP voice compression device adapted to compress the voice data;

audio processing circuitry programmed with an audio processing software application for processing the compressed voice data;

the IP network stack adapted to store and process IP data, the IP network stack including protocols for processing the compressed voice data via an IP network; and

the communication stack adapted to store and process communications data, the communications stack including audio processing protocols for processing the compressed voice data.

15. The telephony communications device of claim 13, wherein the telephony communications device further comprises flash-style, non-volatile memory that includes embedded firmware for that device, and wherein the programmable audio processor chip includes a flash-cache architecture adapted to enable a CPU to boot and run code from the Flash-style, non-volatile memory and mix this execution space with internal memory on the programmable audio processor chip.

16. The telephony communications device of claim 15, further comprising a plurality of communications stacks, wherein the device is adapted to run compute-intensive DSP code

out of the internal memory and to run the communication stacks out of the flash-style, non-volatile memory.

17. The telephony communications device of claim 16, wherein the device is adapted to run the compute-intensive DSP code including at least one of: audio codecs, acoustic echo cancellation and framing.

18. The telephony communications device of claim 16, wherein the communication stacks are adapted to process data for executing at least one of: call setup, call teardown, capabilities exchange and negotiation.

19. (canceled)

20. An IP telephony communications network comprising:

a plurality of IP telephony devices each having a programmable audio processor chip comprising:

a DSP voice compression device adapted to compress the voice data;

audio processing circuitry programmed with an audio processing software application for processing the compressed voice data;

an IP network stack adapted to store and process IP data, the IP network stack including protocols for processing the compressed voice data via an IP network; and

a communication stack adapted to store and process communications data, the communications stack including audio processing protocols for processing the compressed voice data;

a CPU adapted to communicate with the plurality of IP telephony communications devices and to program the programmable audio processor chip in each IP telephony device, the programming including communications protocols, the CPU having a standard RISC 5-stage pipeline adapted to execute a plurality of instructions simultaneously; and

a communications link coupled to each of the IP telephony devices and to the CPU and adapted to transmit communications data including voice IP data.

21. The network of claim 20, wherein the CPU further comprises a DSP Multiply Accumulate (DSPMAC) unit and an Address Generation Unit (AGU).

22. The network of claim 21, wherein the AGU is adapted to effect address calculation concurrently with normal program flow address calculation of the CPU.

23. An IP telephony communications network comprising:

a plurality of IP telephony devices each having a programmable audio processor chip comprising:

a DSP voice compression device adapted to compress the voice data;

audio processing circuitry programmed with an audio processing software application for processing the compressed voice data;

an IP network stack adapted to store and process IP data, the IP data including protocols for processing the compressed voice data via an IP network; and

a communication stack adapted to store and process communications data, the communications data including audio processing protocols for processing the compressed voice data;

a CPU adapted to communicate with the plurality of IP telephony communications devices and to program the programmable audio processor chip in each IP telephony device, the programming including communications protocols, the CPU having a standard RISC 5-stage pipeline adapted to execute a plurality of instructions simultaneously, a DSP Multiply Accumulate (DSPMAC) unit and an Address Generation Unit (AGU), the AGU adapted to effect address calculation concurrently with normal program flow address calculation of the CPU, the DSPMAC and AGU being adapted to be used together in single instruction mnemonics; and

a communications link coupled to each of the IP telephony devices and to the CPU and adapted to transmit communications data including voice IP data.

24. The programmable audio processor chip of claim 1, wherein the IP network stack includes at least one of: a TCP/IP stack and an IP telephony stack.

25. A programmable audio processor chip for processing telephony voice data comprising:

a DSP voice compression and decompression device adapted to compress and decompress the telephony voice data;

a programmable processing layer programmed with an audio processing application for processing the compressed telephony voice data;

an IP network stack adapted to store and process IP telephony data, the IP network stack including protocols for processing the compressed telephony voice data via an IP network; and

a communication stack adapted to store and process communications data, the communications stack including audio processing protocols for processing the compressed voice data.

26. The programmable audio processor chip of claim 25, further comprising an application layer programmed using C programming language.

27. The programmable audio processor chip of claim 26, wherein the application layer is adapted for programming with assembly language.

28. The programmable audio processor chip of claim 25, wherein the DSP voice compression and decompression device is an executable function on the programmable audio processor chip coded as assembly language.

APPENDIX OF EVIDENCE

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.